REMARKS

The Examiner rejected claims 1-2, 9-10, and 17-18 under 35 U.S.C. 103(a) as being unpatentable over Karlsson et al. (newly cited US 7,269,175) in view of the background of Takada et al. (newly cited US 6,850,520) and Lee (newly cited US 2003/0088685). Applicant submits that as currently amended, claims 1-2, 9-10, and 17-18 are not obvious in view of the cited prior art.

Claim 1 has been amended to explicitly require the real-time reassembly of *frames* of ATM data, that the index corresponding to each ATM cell is placed in the circular buffer and is used by the plurality of parallel processors to determine a cell type, and the parallel processors determine the AAL mode if any of each cell.

Regarding claim 1, the Examiner looks to Figure 4 of Karlsson as disclosing a system comprising a circular buffer for storing ATM data. In particular the Examiner points to the FIFOs shown in that figure. The Examiner maintains that fifos are interchangeable with circular buffers, since a fifo with it head and tail linked is a circular buffer. The Examiner also looks to Karlsson as teaching ATM data comprising information divided into ATM cells (see column 2, lines 13+, ATM uses fixed length cells), the ATM cells comprising at least one of virtual path identifier (VPI) information, virtual channel identifier (VCI) and channel identifier (CID) information (see column 11, lines 56-58, channel identifier in AAL packet), and a content addressable memory configured to receive any of the VPI, VCI and CID information related to each ATM cell and configured to provide an index when particular VPI, VCI and CID information is identified, the index corresponding to unique VPINCI and VPINCI+CID combinations, the index placed in the circular buffer and used to determine an AAL mode of each ATM cell (see figure 5 and column 11, line 56 to column 12, line 18, the channel identifier (CID) is used to find the entry in the look up table, the entry having an index showing as active, so that the AAL packet can be forwarded to the FIF0s).

The Examiner admits that Karlsson does not explicitly teach a plurality of parallel processing elements configured to analyze the ATM cells and determine a cell type.
The Examiner argues that claimed limitation is well known in the art, as evidenced by Takada. In particular, Takada teaches a plurality of parallel processing elements (see column

2, lines 32-45, parallel processing of ATM cells) configured to analyze the ATM cells and determine a cell type (see column 2, lines 32-45, each cell processor is provided with a cell identifying section that determines and the cell type from the header information). The Examiner maintains that it would have been obvious to a person having ordinary skill to modify the system of Karlsson as taught by Takada, since Takada stated that the various OAM cell types can be used to quickly detect failures and changes in quality.

The Examiner admits that Karlsson and Takada do not explicitly teach that the ATM adaptation layer 2 cells and AAL 5 cells are reassembled in real time. The Examiner looks to lee as teaching the cell type and that cells are reassembled in real time, the motivation for combining the teachings being to maintain quality of service.

Claim 1 requires a circular buffer for storing ATM data. The Examiner points to Karlsson, Figure 4, stating that the SAR channel FIFOs 410 "are easily interchangeable with circular buffers where the head and tail are linked". In essence, the Examiner is arguing that one of ordinary skill would be led to replace the FIFO buffers of Karlsson with circular buffers. The Examiner does not provide any motivation for making this change.

First, Applicant submits that although the head and tail of a FIFO may indeed be linked to form a circular buffer, a circular buffer and a FIFO buffer are not equivalent or interchangeable. A circular buffer is a memory in which the address of the next storage location that is to be used to store data is (I+1) mod N, where I is the last location that was used to store data and N is the size of the buffer. A FIFO is a buffer in which data is removed in the order it was received. Data is input at a particular location and removed at another location. Data is only removed from a FIFO at the this removal location. A FIFO buffer is equivalent to shift register. A circular buffer places no constrains on the order in which data is removed. In fact, data can be accessed simultaneously from a plurality of locations within the buffer, a property that utilized in the present invention but has no value in the system of Karlsson. Hence, a FIFO and a circular buffer are not interchangeable.

Second, replacing the FIFOs of Karlsson with circular buffers would not provide any advantage in the apparatus taught therein. In fact, the suggested modification would actually require additional hardware to keep track of the oldest entry that has not been overwritten or

outputted. Neither Takada nor Lee provide the teachings of a circular buffer, missing from Karlsson.

Claim 1 also requires a content addressable memory (CAM) configured to receive any of the VPI, VCI and CID information related to each ATM cell and configured to provide an index when particular VPI, VCI and CID information is identified, the index corresponding to unique VPI/VCI and VPI/VCI+CID combinations, wherein the index is placed in the circular buffer. The Examiner points to Karlsson (Figure 5 and column 11, line 56 to column 12 line 18) as providing this teaching. The cited passage relates to Figure 4 rather than Figure 5, so Applicant has carefully considered both Figures as well as the cited passage in responding to the Examiner's rejection.

First, Applicant finds no teaching of any **content addressable memory** in the cited passage or in either Figure 4 or Figure 5. Second, Applicant finds no teaching in the cited passage or elsewhere in Karlsson regarding the provision of any index **corresponding to unique VPI/VCI and VPI/VCI+CID combinations** or the placing of such an index in the SAR channel FIFOs 410 of Figure 4, identified by the Examiner as equivalent to circular buffers.

At most, Karlsson teaches (column 12, lines 8-18) that a channel identifier CID is used to keep track of the origins of the data so that correct interleaving of the data packets may be carried out. The channel identifier is not an index corresponding to unique VPI/VCI and VPI/VCI+CID combinations as required by the claim. Hence, Applicant disagrees with the Examiner's reading of Karlsson as teaching either the content addressable memory or the provision of the index. Neither Takada nor Lee provides the missing teaching.

As currently amended, claim 1 requires a plurality of parallel processing elements configured to analyze the ATM cells, to determine a cell type using the index, and to determine the ATM adaption layer (AAL) mode if any of each cell.

First, as noted above, Karlsson does not teach an index as required, so it could not teach the use of the index to determine a cell type. Second, there is no teaching in Karlsson

of determining the AAL mode, let alone that the determining is carried out by a plurality of processing elements. Third, as the system taught by Karlsson, the primary cited reference, is directed towards the interleaving of AAL2 cells from one sub-system with signaling and management packets from another subsystem, the type of each cell and its AAL mode if any would be known *a priori* and there would be no obvious benefit to that system in re-determining the type and mode.

Finally, as currently amended, claim 1 requires the real time reassembly of AAL2 and AAL5 cells into frames of ATM data. The only teaching in Karlsson regarding real-time data is in the context of assigning higher priority to connections carrying real-time data than to those carrying non-real-time data (column 14, lines 58-65). Takada does not mention any real-time data processing. The teachings of Lee are directed towards (Abstract, paragraph 21, Figures 4 and 5) a system that deals with traffic congestion or link failure by (1) **converting** incoming AAL5 traffic into AAL2 traffic, then giving real-time AAL2-traffic priority for ongoing transmission and (2) **converting** incoming AAL2 traffic into AAL5 traffic, then giving real-time AAL5-traffic priority for ongoing transmission. In other words, Lee teaches that high priority "real-time" cells of either AAL2 or AAL5 types may be converted into cells of the opposite type and then given priority over other traffic. At most, this amounts to teaching that some AAL2 and AAL5 cells may be transmitted, in a converted form, through the system with "real time" priority over other cells. This is not equivalent to teaching that the AAL2 and AAL5 cells are **reassembled in real time into the frames of ATM data** as the claim requires. Hence, Applicant submits that Lee does not provide the reassembly teachings that are missing from Karlsson and Takada. Accordingly, Applicant submits that as currently amended, claim 1 and the claims dependent therefrom are not obvious in view of the cited prior art.

Claim 2 depends from claim 1 and further requires that the circular buffer communicate with the plurality of parallel processing elements simultaneously. The Examiner states that Karlsson does not provide this additional teaching, but states that this is well known in the art, pointing to Takada. (figure 4 and column 2, lines 27+). The Examiner maintains that it would have been obvious to modify the method of Karlsson as taught by Takada "to quickly detect failures and changes in quality". Applicant submits that even if the

FIFOs of Karlsson were to be replaced by circular buffers, there would be no obvious benefit to Karlsson in providing simultaneous communication access from each of those buffers to a plurality of parallel processing elements, since the system is configured to access the data in those buffers sequentially. Hence, there are additional grounds for allowing claim 2.

Claim 9 has been amended in a similar way to claim 1. Claims 9 and 10 are method claims, with limitations corresponding in method form to the system limitations of claims 1 and 2. Applicant refers the Examiner to above arguments with respect to claims 1 and 2. In brief, as noted above with respect to claim 1, the cited prior art does not teach the use of the circular buffer, the content addressable memory, the existence or use of the index, determining the AAL mode if any of each cell, or the real time reassembly of AAL2 and AAL5 cells into frames of ATM data. Hence, Applicant submits that as currently amended, claim 9 and the claims dependent therefrom are not obvious in view of the cited prior art. Furthermore, there are the same additional grounds for allowing claim 10 as those noted above with respect to claim 2.

Claim 17 has been amended in a similar way to claims 1 and 9. Claims 17 and 18 concern computer program logic, with specific limitations corresponding to the limitations of claims 1 and 2. Applicant refers the Examiner to above arguments with respect to claims 1 and 2. In brief, as noted above with respect to claim 1, the cited prior art does not teach the use of the circular buffer, the content addressable memory, the existence or use of the index, determining the AAL mode if any of each cell, or the real time reassembly of AAL2 and AAL5 cells into frames of ATM data. Hence, Applicant submits that as currently amended, claim 17 and the claims dependent therefrom are not obvious in view of the cited prior art. Furthermore, there are the same additional grounds for allowing claim 18 as those noted above with respect to claim 2.

Claims 3-4, 11-12, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karlsson in view of Takada and Lee as applied to claims 2, 10 and 18 above, and further in view of Suzuki et al. (previously cited US 6,687,250). Applicant submits that as currently amended, claims 3-4, 11-12, and 19-20 are not obvious in view of the cited prior art.

Claims 3-4, 11-12 and 19-20 depend from claims 1, 9 and 17 respectively. The Examiner looks to the combination of Karlsson, Takada and Lee as teaching the base claim limitations and to Suzuki for the additional teachings required by these dependent claims.

Applicant submits that as noted above with respect to claims 1, 9, and 17, the combination of Karlsson, Takada and Lee does not teach all the requirements of the base claims. In brief, the cited prior art does not teach the use of the circular buffer, the content addressable memory, the existence or use of the index, determining the AAL mode if any of each cell, or the real time reassembly of AAL2 and AAL5 cells into frames of ATM data. Suzuki does not provide the missing teachings. Hence, Applicant submits that as currently amended, claims 3-4, 11-12 and 19-20 are not obvious in view of the cited prior art.

Claims 5-8, 13-16 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karlsson in view of Takada, Lee and Suzuki as applied to claims 4, 12 and 20 above, and further in view of VanDervort et al. (previously cited US 5,761,191). Applicant submits that as currently amended, claims 5-8, 13-16 and 21-24 are not obvious in view of the cited prior art.

Claims 5-8, 13-16 and 21-24 depend from claims 4, 12 and 20 respectively. The Examiner looks to the combination of Karlsson, Takada, Lee and Suzuki as teaching the limitations of claims 4, 12 and 20 respectively and to VanDervort for the additional teachings required by dependent claims 5-8, 13-16 and 21-24.

Applicant submits that as noted above with respect to claims 4, 12, and 20, the combination of Karlsson, Takada Lee and Suzuki does not teach all the requirements of the base claims 1, 9 and 17 from which claims 4, 12, and 20 in turn depend . In brief, the cited prior art does not teach the use of the circular buffer, the content addressable memory, the existence or use of the index, determining the AAL mode if any of each cell, or the real time reassembly of AAL2 and AAL5 cells into frames of ATM data. VanDervort does not provide the missing teachings. Hence, Applicant submits that as currently amended, claims 5-8, 13-16 and 21-24 are not obvious in view of the cited prior art.

Respectfully Submitted,

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Date: September 2, 2009

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